IN THE CLAIMS

1. (Currently Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a plurality of circuit elements formed in an element forming layer on said semiconductor substrate;

a plurality of first and second terminals formed on the surface of said element forming layer and connected to predetermined ones of said circuit elements;

a plurality of conductive layers which are respectively connected to said first terminals ~~corresponding to some terminals of said plurality of terminals~~ and extending on said element forming layer;

protruding electrodes respectively connected to said conductive layers;

testing pads respectively connected to said second terminals, said testing pads being not coupled to any protruding electrode; and

an insulating film which covers the surfaces of said protruding electrodes and said testing pads so as to expose said protruding electrodes and said testing pads.

2. (Previously Presented) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a plurality of circuit elements formed in an element forming layer on said semiconductor substrate;

first and second terminals formed on the surface of said element forming layer and connected to predetermined ones of said circuit elements;

a conductive layer which is connected to said first terminal;

a protruding electrode connected to said conductive layer;

a testing pad connected to said second terminal, said testing pad being not coupled to any protruding electrode; and

an insulating film which covers the surfaces of said protruding electrode and said testing pad so as to expose said protruding electrode and said testing pad.

3. (Previously Presented) The semiconductor integrated circuit device according to claim 1, wherein said conductive layers are metal wirings, said insulating film is formed on said each metal wiring, and an insulating film is further formed below said each metal wiring.

4. (Original) The semiconductor integrated circuit device according to claim 3, wherein said insulating film and said further insulating film are respectively formed of different materials, and said insulating film is formed of a material higher in elastic modulus than said further insulating film.

5. (Previously Presented) The semiconductor integrated circuit device according to claim 3, wherein said insulating film is a film which contains an organic substance.

6. (Original) The semiconductor integrated circuit device according to claim 5, wherein the film containing the organic substance is a polyimide film, a fluorocarbon resin film, or an elastomer film which contains a silicon or acrylic rubber material.

7. (Previously Presented) The semiconductor integrated circuit device according to claim 1, wherein said testing pads are placed just above said terminals corresponding thereto.

8. (Original) The semiconductor integrated circuit device according to claim 7, wherein said testing pads are regularly placed in the central portion of said semiconductor substrate, and said protruding electrodes are regularly placed outside said testing pads respectively.

9. (Previously Presented) The semiconductor integrated circuit device according to claim 3, wherein said testing pads extend on said further insulating film.

Claims 10-22 (Canceled)

23. (Previously Presented) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a first circuit element and a second circuit element formed on said semiconductor substrate;

a wiring formed over said semiconductor substrate and connected to said first circuit element;

a bump formed over said wiring and connected thereto; and

a conductive layer, which is formed over said semiconductor substrate and connected to said second circuit element and which constitutes a testing pad,

wherein said conductive layer is electrically isolated from any bump.

24. (Previously Presented) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a semiconductor integrated circuit element formed in said semiconductor substrate;

a wiring formed on said semiconductor substrate and connected to said semiconductor integrated circuit element;

a bump formed on said wiring and connected thereto; and

a conductive layer, which is formed on said semiconductor substrate and connected to said semiconductor integrated circuit element and which constitutes a testing pad which is electrically isolated from any bump,

wherein when said semiconductor integrated circuit element is tested, said testing pad is electrically connected to the outside of said semiconductor integrated circuit device, and

when said semiconductor integrated circuit element is in normal operation, said testing pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

25. (Previously Presented) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

integrated circuit elements formed on said semiconductor substrate;

a plurality of wirings formed on said semiconductor substrate and connected to said integrated circuit elements;

a plurality of bumps formed on said plurality of wirings and provided in association with said plurality of wirings;

a conductive layer, which is formed on said semiconductor substrate and connected to said integrated circuit elements and which is formed as a testing pad which is electrically isolated from any bump; and

an organic film placed on said semiconductor substrate and formed below said plurality of wirings,

wherein when said each integrated circuit element is tested, each said testing pad is electrically connected to the outside of said semiconductor integrated circuit device, and

when each said integrated circuit element is in normal operation, each said testing pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

26. (Previously Presented) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a first circuit element and a second circuit element formed on said semiconductor substrate;

a wiring formed on said semiconductor substrate and connected to said first circuit element;

a bump formed on said wiring and connected thereto;

a first conductive material, which is formed on said semiconductor substrate and connected to said first circuit element and which constitutes a first testing pad; and

a second conductive material, which is formed on said semiconductor substrate and connected to said second circuit element and which constitutes a second testing pad which is not connected to any bump,

wherein when said first circuit element and said second circuit element are tested, said first testing pad and said second testing pad are electrically connected to the outside of said semiconductor integrated circuit device, and

when said first circuit element and said second circuit element are in normal operation, said first testing pad is electrically connected to the outside of said semiconductor

integrated circuit device through said bump, and said second testing pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

27. (Previously Presented) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

an integrated circuit formed on said semiconductor substrate;

a wiring formed on said semiconductor substrate and connected to said integrated circuit;

a bump formed on said wiring and connected thereto;

a first conductive layer, which is formed on said semiconductor substrate and connected to said integrated circuit and which constitutes a first testing pad; and

a second conductive layer, which is formed on said semiconductor substrate and connected to said integrated circuit and which constitutes a second testing pad which is not connected to any bump,

wherein said first conductive layer and said wiring are connected to each other, and

when said integrated circuit is tested, said first testing pad and said second testing pad are electrically

connected to the outside of said semiconductor integrated circuit device and

when said integrated circuit is in normal operation, said first testing pad is electrically connected to the outside of said semiconductor integrated circuit device and said second testing pad is electrically isolated from the outside of said semiconductor integrated circuit device.

28. (Previously Presented) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

integrated circuit elements formed on said semiconductor substrate;

a plurality of wirings formed over said semiconductor substrate and connected to at least one of said integrated circuit elements;

a plurality of bumps formed over said plurality of wirings and provided in association with said plurality of wirings;

a conductive layer, which is formed over said semiconductor substrate and connected to at least one of said integrated circuit elements and which constitutes a test pad which is not connected to any bump; and

a film containing an organic material formed between said semiconductor substrate and said plurality of wirings and between said semiconductor substrate and said conductive layer,

wherein when said integrated circuit element is tested, said test pad is electrically connected to the outside of said semiconductor integrated circuit device, and

when said integrated circuit element is in normal operation, said test pad is electrically disconnected from the outside of said semiconductor integrated circuit device.